SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]

CIT Campus, MGR Knowledge City, Taramani,

Chennai – 600 113, India.

Advertisement No. SETS/Chn/Rec/Proj/2020-21/02 Date : 22nd March 2021

Society for Electronic Transactions and Security [SETS] is a non-profit society dedicated to research and development in the field of Cyber Security.

SETS invites applications from citizens of India for filling up the position of **Project Associate – III and Project Associate – II** for a Research & Development project in the area of Quantum Key distribution for a project titled "**: Metro Area Quantum Access Network (MAQAN)**".

Short description of the project: Metro Area Quantum Access Network (MAQAN) ensures secure key exchange between point-multipoint using Quantum mechanisms. In this project, SETS focus would be on developing efficient post processing module required for field-deployable QKD systems. The post processing module includes interfacing with quantum components, sifting, error parameter estimation, clock synchronization, authentication, privacy amplification, error correction, error verification, along with Quantum-safe Post Quantum Crypto primitives.

The descriptions of positions, detailed qualification requirements and salary are given below:

1. Qualification requirements for the post Project Associate – III

Name of the Post	**Project Associate - III**
Number of Posts	**One**
Age Limit	Not more than **35 years** as on
Essential Qualification	i. PhD in Engineering/ Science (Physics/Electronics) or ii. First Class M. Tech /M. E (Microelectronics and Photonics/Laser and Electro optics/Applied Electronics/VLSI Design/Electronic & Instrumentation/ Communication System/ Computer Science/ Cyber-Security)
Experience	MTech/ ME with minimum two years' experience (or) PhD in Science with minimum one year experience (or) PhD in Engineering
Relevant Work Experience	Candidates with experience in Quantum Key Distribution, Integration of Optoelectronic Hardware with FPGA, Post Quantum Cryptography, Quantum Network testbed creation and System Design & Development using FPGAs.
Areas of Skill sets / Knowledge required	a) Knowledge of Quantum Key Distribution protocols, high speed optical communication protocols (10Gig Ethernet, IBERT).

	b) Knowledge of Post Quantum Cryptography (Digital Signature and Key Exchange protocols) c) Knowledge of Quantum Network testbed creation and protocols testing d) Hands-on exposure of FPGA boards and Xilinx Vivado tools using Verilog/VHDL/HLS. Integration of optical and classical components
Remuneration	Consolidated salary would be in the range of Rs**. 50,000 to 60,000 per month based on the experience and profile.**

2. Qualification requirements for the post Project Associate – II

Name of the Post	**Project Associate - II**
Number of Posts	**One**
Age Limit	Not more than **35 years** as on
Essential Qualification	i. PhD in Engineering/ Science (Physics/Electronics) (or) ii. First Class M. Tech /M. E (Microelectronics and Photonics/Laser and Electro optics/Applied Electronics/VLSI Design/ Communication System/ Computer Science/Cyber-Security)
Experience	MTech/ M.E with minimum one year experience (or) PhD in Science (or) PhD in Engineering.
Work Experience / Desirable criteria	Candidates with experience in Quantum Key Distribution, Integration of Optoelectronic Hardware with FPGA, Post Quantum Cryptography, Quantum Network testbed creation and System Design & Development using FPGAs.
Areas of Skill sets/ Knowledge required	a) Knowledge of Quantum Key Distribution, Post Quantum Cryptography (Digital Signature and Key Exchange protocols) b) Hands-on exposure on high-speed ADC-DAC, Time-to Digital convertors implementations on FPGA, optoelectronics. c) Hands-on exposure of Xilinx Vivado tools, FPGA designs using Verilog/VHDL and HLS. Languages Python, C and C++
Remuneration	Consolidated salary would be **Rs. 40,000 per month**

The positions (Project Associate – II and Project Associate – III) as proposed are purely temporary and would be filled on a contract basis with a consolidated salary under project mode. The duration of the assignment is initially for a period of One Year and would be extended further till end of the project based on the performance. There is no scope of continuation/regularization/absorption under any circumstances.

Application Procedure:

1. **Only applications received via email will be considered**. The Subject line in the email should contain the "**Application for the post of <u>Project Associate – III / Project Associate - II</u>**". The candidate is required to attach the following documents to the Email:

   a. Resume (doc/pdf format) and

   b. Personal Particulars form (pdf format) duly filled.

   The Personal Particulars form is hosted at SETS homepage **https://setsindia.in/.**
2. The email should be sent to **hr_qkd2_2021(at)setsindia.net.**
3. **The last date for receiving applications by Email is 5th April 2021.**
4. Shortlisted candidates would be required to attend a Written Test and/or Interview at SETS, Chennai. The date and time for this would be intimated to shortlisted candidates by Email.

Terms and Conditions:

1. The shortlisted candidates would be required to bring all their original testimonials for verification on the test/interview day.
2. No TA/DA will be given to candidates appearing for written test or interview.
3. The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications, cancellation of advertisement and filling up or not filling up of post will be final and no inquiry or correspondence will be entertained in this matter.

Executive Director