



**SOCIETY FOR ELECTRONIC TRANSACTIONS AND SECURITY [SETS]**  
CIT Campus, MGR Knowledge City, Taramani, Chennai – 600 113, India.

**Advertisement No. SETS/Chn/Rec/Proj/2023-24/15 Date : 6<sup>th</sup> September 2023**

**Society for Electronic Transactions and Security [SETS]** is a Society under Societies Registration Act, XXI of 1860, dedicated to carry-out Research and Development in the field of Information Security focusing on the key verticals, namely, Cryptology and Computing, Hardware Security, Quantum Security and Network Security.

SETS invites applications from citizens of India for filling up the following positions for a Research & Development project in the area of Cybersecurity.:

- 1. Project Scientist (Consultant Mode) - 1 Position (Hardware)**
- 2. Project Associate - 3 Positions (Hardware)**

**The descriptions of positions, detailed qualification requirements and salary are given below:**

- 1. Project Scientist (Consultant Mode) (Hardware)**

<b>Name of the Post</b>	<b>Project Scientist (Consultant Mode) (Hardware)</b>
<b>Number of Posts</b>	One
<b>Age Limit</b>	Not more than 35 years as on 20.09.2023
<b>Qualification</b>	First Class M.Tech /M.E (Computer Science/ Information Security/Cyber Security/Network Security/ Embedded Systems/ Communication Systems/ VLSI Design/ Electronic Engineering)
<b>Desirable Qualification</b>	PhD in Embedded Systems/Electronics / Communication Engineering /Computer Science/ Cyber security/Network Security / InformationSecurity /IoT
<b>Areas of Skill sets/ Knowledge required</b>	a) Hands-on experience in Xilinx Vivado tools, simulation using MATLAB / ModelSim and FPGA realization using VHDL/Verilog programming. b) Programming Experience in C and Python c) Knowledge in Digital Electronics d) Knowledge in Artificial Intelligence e) Knowledge in Hardware Security/ Side Channel Analysis
<b>Experience</b>	5 Years of R&D Experience in Cyber Security in the area of VLSI/ Embedded Systems/ Artificial Intelligence/ Side Channel Analysis Equivalent work experience in lieu of higher degree:  - Engineering Doctorates: Four years
<b>Remuneration</b>	Consolidated salary of Rs.80,000 per month, additional increments may be given based on skill sets and relevant experience of candidate. (based on performance of the first year 5-8% increment may be considered)

## 2. Project Associate (Hardware)

<b>Name of the Post</b>	<b>Project Associate (Hardware)</b>
<b>Number of Posts</b>	Three
<b>Age Limit</b>	Not more than 35 years as on 20.09.2023
<b>Qualification</b>	First Class B.E / B.Tech ECE/EEE/E&I/CSE/IT/ICT
<b>Desirable Qualification</b>	First Class M.Tech /M.E / MS by Research (Embedded Systems/Communication Systems/VLSI Design/ Electronic Engineering / Computer Science/Cyber security/Network Security)
<b>Areas of Skill sets/ Knowledge required</b>	a) Hands-on experience in Xilinx Vivado tools, simulation using MATLAB / ModelSim and FPGA realization using VHDL/Verilog programming. b) Knowledge in Digital Electronics c) Knowledge in Cryptography d) Knowledge in Hardware Security/ Side Channel Analysis
<b>Experience</b>	2 to 4 Years of Relevant Experience  Equivalent work experience in lieu of higher degree: - Engineering Post-Graduates: Two years - Engineering Doctorates: Four years
<b>Remuneration</b>	Consolidated salary would be Rs.40,000-50,000/- per month, additional increment may be given based on the skill sets and relevant experience of candidate.

The positions of Project Scientists (Consultant Mode) & Project Associates as proposed is purely temporary and would be filled on a contract basis with a consolidated salary underproject mode. The duration of the assignment is initially for a period of One Year and would be extended further based on the need of the project and performance with an increment up to 8% may be considered. There is no scope of continuation/regularization/absorption under any circumstances.

### Application Procedure:

- Only applications received via Google Form will be considered. The Candidate should choose the appropriate post to apply (“Project Scientist (Consultant Mode)/ Project Associate (Hardware)”).** Please find below the link for the Google form:

Name of the Post	Google Form Link
1. Project Scientists (Consultant Mode) (Hardware)	<a href="https://forms.gle/vAGDWFY471jAVyWh6">https://forms.gle/vAGDWFY471jAVyWh6</a>
2. Project Associate (Hardware)	<a href="https://forms.gle/hwBgmtRq66g11G1J7">https://forms.gle/hwBgmtRq66g11G1J7</a>

- The candidate is requested to attach the following documents:-
  - Scanned copy of Personal Particulars form (pdf format) duly filled and signed. The Personal Particulars form is available at SETS homepage <https://setsindia.in/careers>
  - Scanned copies of certificates of Academic Qualifications (Single PDF document)
  - Scanned copies of Experience certificates (Single PDF document)
- The last date for uploading applications via Google Form is 20.09.2023.
- Shortlisted candidates would be required to attend a Written Test and/or Interview at SETS, Chennai. The date and time for this would be intimated to shortlisted candidates by E-mail.

**Terms and Conditions:**

1. The shortlisted candidates would be required to bring all their original testimonials for verification on the interview day.
  2. No TA/DA will be given to candidates appearing for interview.
  3. The prescribed qualifications are minimum and mere possession of the same does not entitle the candidate to be called for the written test or interview. The decision of the Executive Director of SETS in all matters relating to eligibility, acceptance or rejection of the applications, cancellation of advertisement and filling up or not filling up of post will be final and no inquiry or correspondence will be entertained in this matter.
  4. Number of vacancies may increase/decrease depending upon SETS requirements and such changes will be made by SETS without any notice.
- ❖ In case of any queries/issues related to uploading the form may please be intimated via email id: [hrd2023-02-proj@setsindia.net](mailto:hrd2023-02-proj@setsindia.net)

**Executive Director**